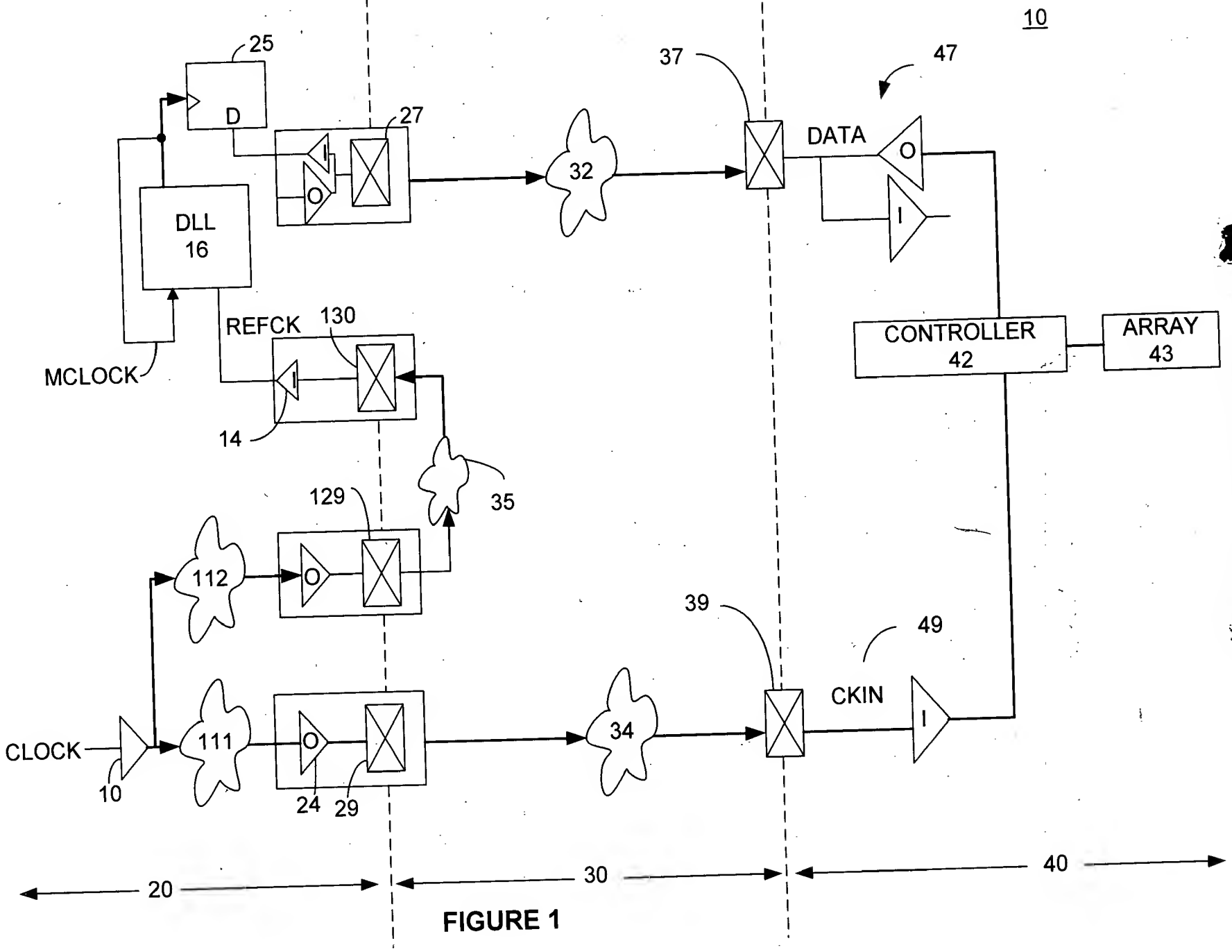
10
25
D
27
I
O
DLL
16
MCLOCK
REFCK
130
I
14
35
129
112
O
37
47
32
DATA
O
I
CONTROLLER
42
ARRAY
43
39
49
CKIN
I
CLOCK
10
111
O
24
29
34
20
30
40

FIGURE 1

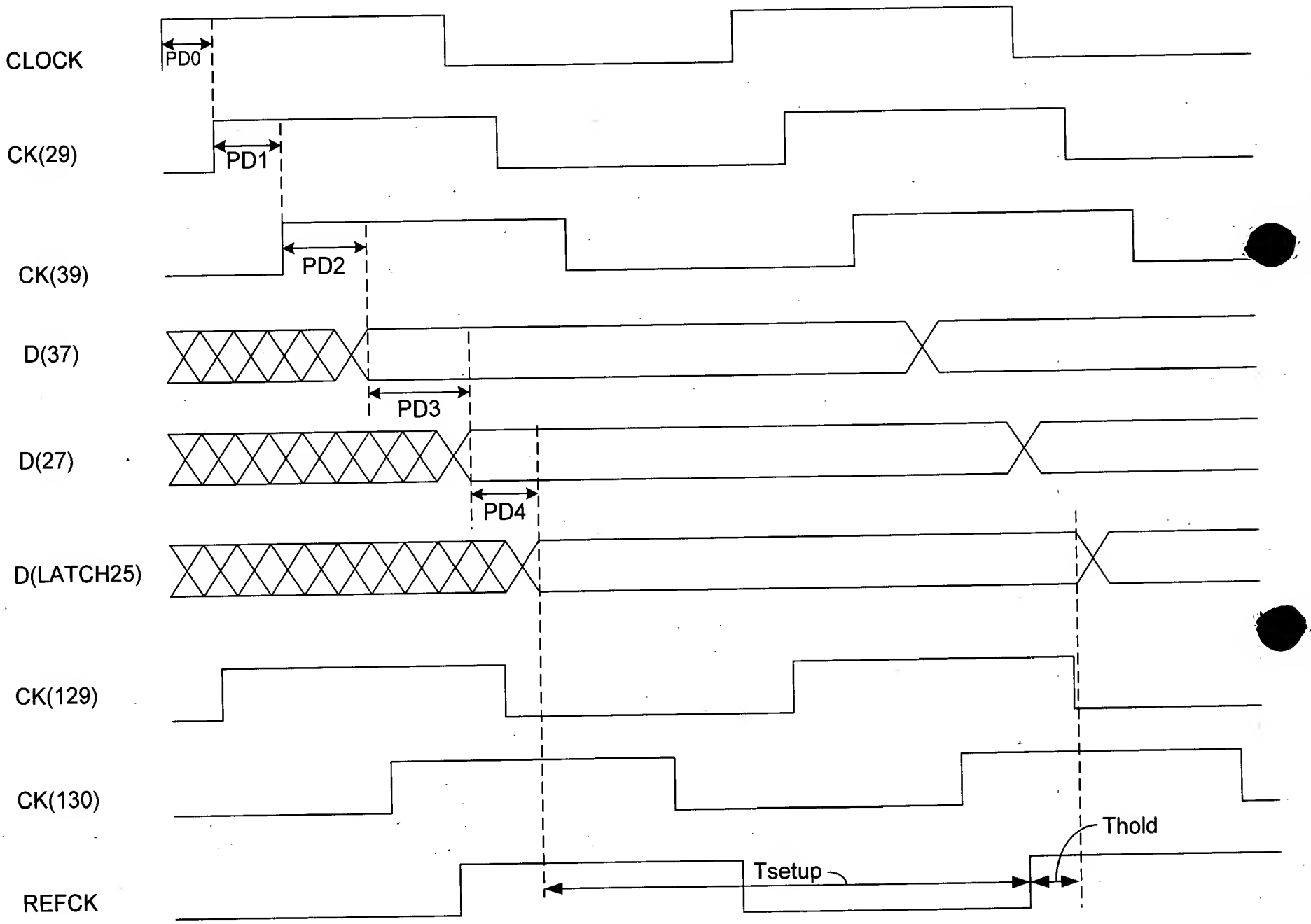
CLOCK
PD0
CK(29)
PD1
CK(39)
PD2
D(37)
PD3
D(27)
PD4
D(LATCH25)
CK(129)
CK(130)
Thold
Tsetup
REFCK

FIGURE 2

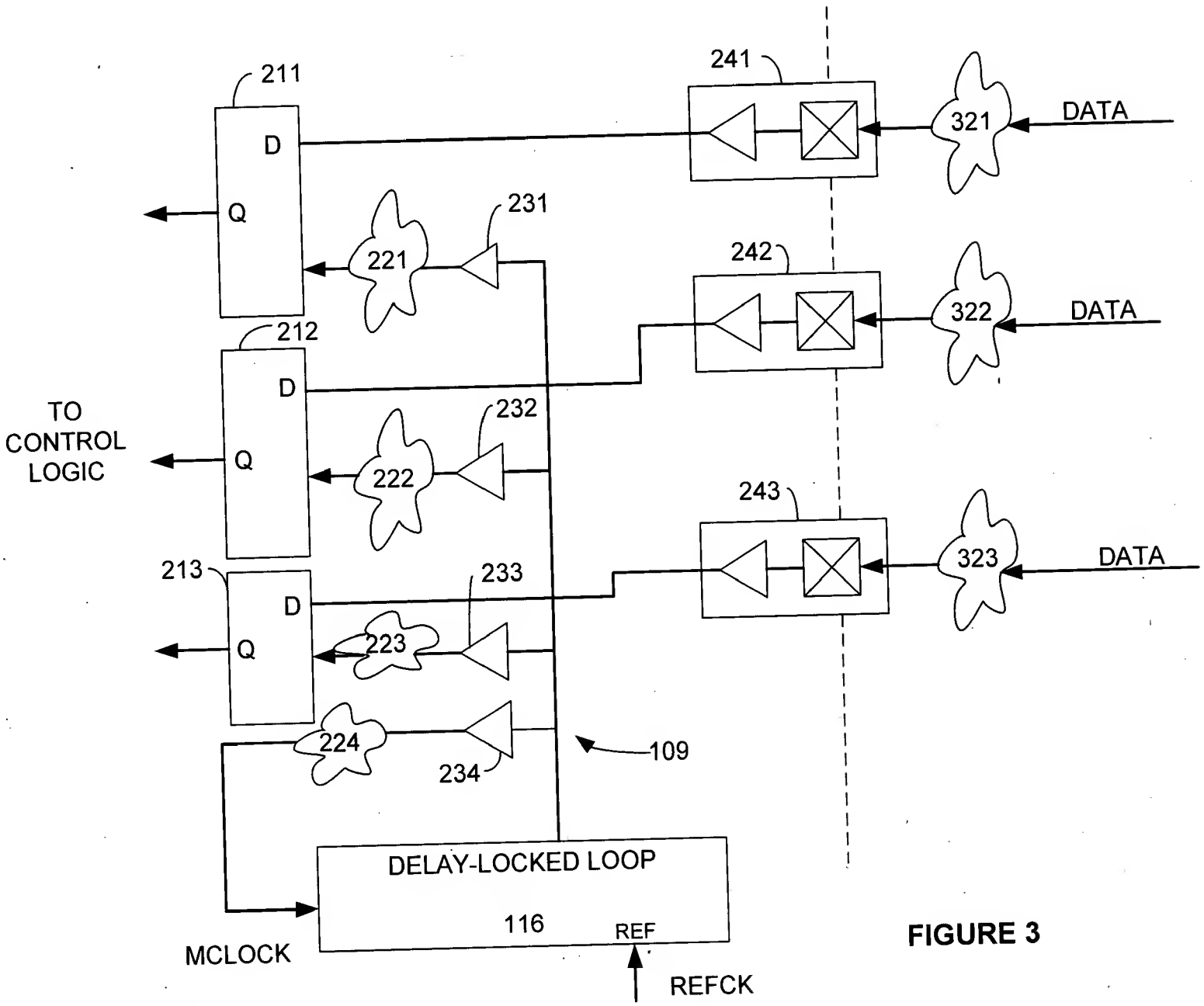
211
D
Q
241
321
DATA
231
221
242
322
DATA
212
D
Q
TO
CONTROL
LOGIC
232
222
243
323
DATA
213
D
Q
233
223
224
234
109
DELAY-LOCKED LOOP
116
REF
MCLOCK
REFCK

FIGURE 3

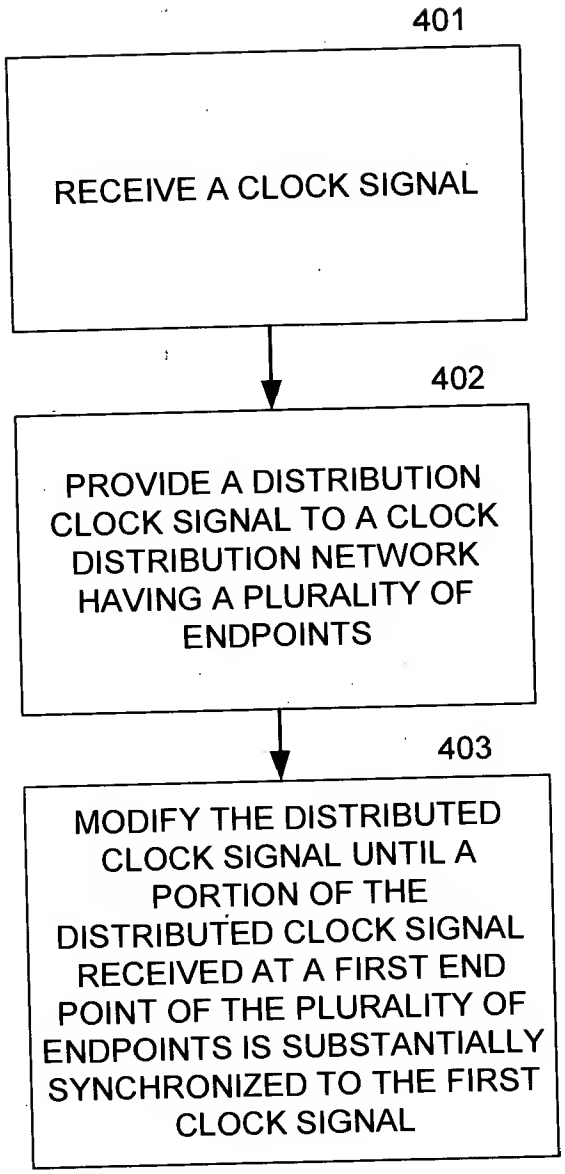
401
RECEIVE A CLOCK SIGNAL
402
PROVIDE A DISTRIBUTION CLOCK SIGNAL TO A CLOCK DISTRIBUTION NETWORK HAVING A PLURALITY OF ENDPOINTS
403
MODIFY THE DISTRIBUTED CLOCK SIGNAL UNTIL A PORTION OF THE DISTRIBUTED CLOCK SIGNAL RECEIVED AT A FIRST END POINT OF THE PLURALITY OF ENDPOINTS IS SUBSTANTIALLY SYNCHRONIZED TO THE FIRST CLOCK SIGNAL

FIGURE 4

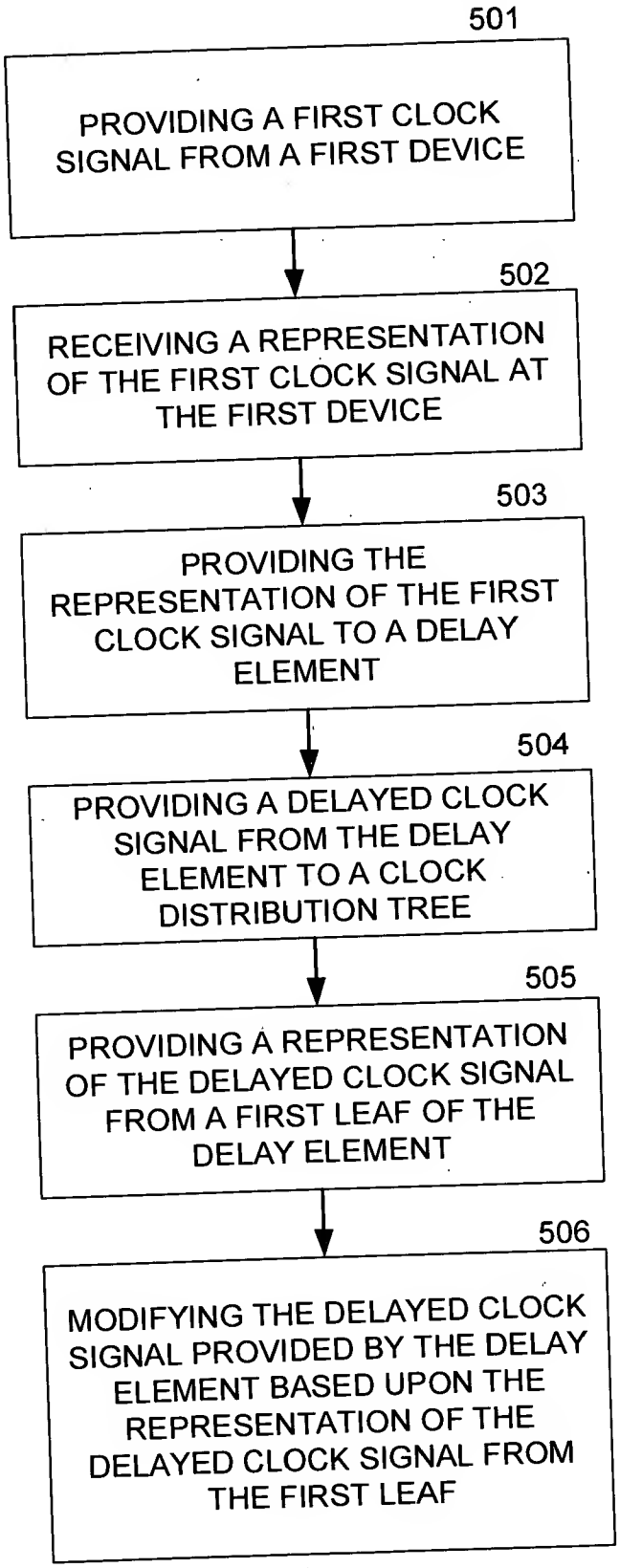
501
PROVIDING A FIRST CLOCK SIGNAL FROM A FIRST DEVICE
502
RECEIVING A REPRESENTATION OF THE FIRST CLOCK SIGNAL AT THE FIRST DEVICE
503
PROVIDING THE REPRESENTATION OF THE FIRST CLOCK SIGNAL TO A DELAY ELEMENT
504
PROVIDING A DELAYED CLOCK SIGNAL FROM THE DELAY ELEMENT TO A CLOCK DISTRIBUTION TREE
505
PROVIDING A REPRESENTATION OF THE DELAYED CLOCK SIGNAL FROM A FIRST LEAF OF THE DELAY ELEMENT
506
MODIFYING THE DELAYED CLOCK SIGNAL PROVIDED BY THE DELAY ELEMENT BASED UPON THE REPRESENTATION OF THE DELAYED CLOCK SIGNAL FROM THE FIRST LEAF

FIGURE 5

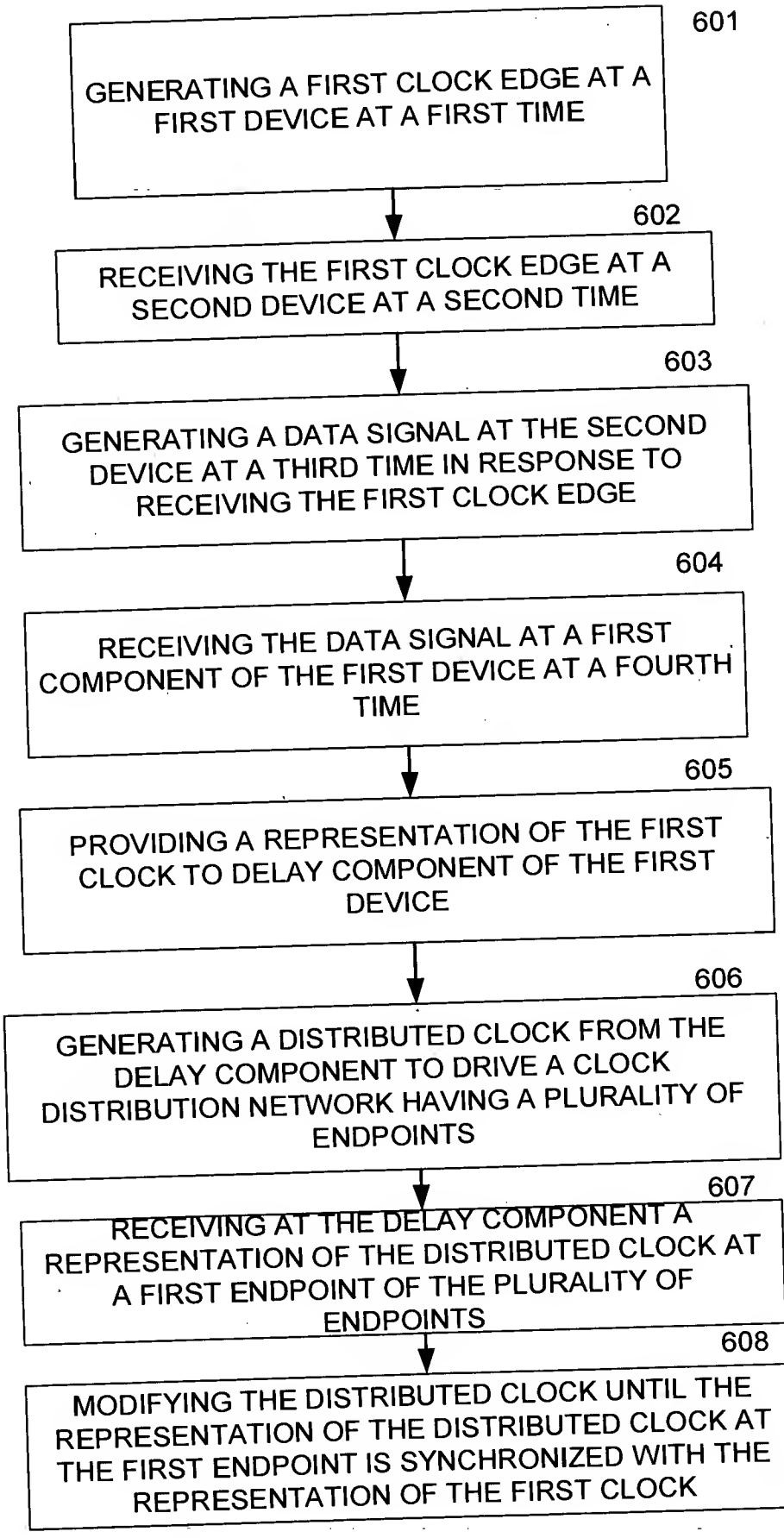
601
GENERATING A FIRST CLOCK EDGE AT A FIRST DEVICE AT A FIRST TIME
602
RECEIVING THE FIRST CLOCK EDGE AT A SECOND DEVICE AT A SECOND TIME
603
GENERATING A DATA SIGNAL AT THE SECOND DEVICE AT A THIRD TIME IN RESPONSE TO RECEIVING THE FIRST CLOCK EDGE
604
RECEIVING THE DATA SIGNAL AT A FIRST COMPONENT OF THE FIRST DEVICE AT A FOURTH TIME
605
PROVIDING A REPRESENTATION OF THE FIRST CLOCK TO DELAY COMPONENT OF THE FIRST DEVICE
606
GENERATING A DISTRIBUTED CLOCK FROM THE DELAY COMPONENT TO DRIVE A CLOCK DISTRIBUTION NETWORK HAVING A PLURALITY OF ENDPOINTS
607
RECEIVING AT THE DELAY COMPONENT A REPRESENTATION OF THE DISTRIBUTED CLOCK AT A FIRST ENDPOINT OF THE PLURALITY OF ENDPOINTS
608
MODIFYING THE DISTRIBUTED CLOCK UNTIL THE REPRESENTATION OF THE DISTRIBUTED CLOCK AT THE FIRST ENDPOINT IS SYNCHRONIZED WITH THE REPRESENTATION OF THE FIRST CLOCK

FIGURE 6

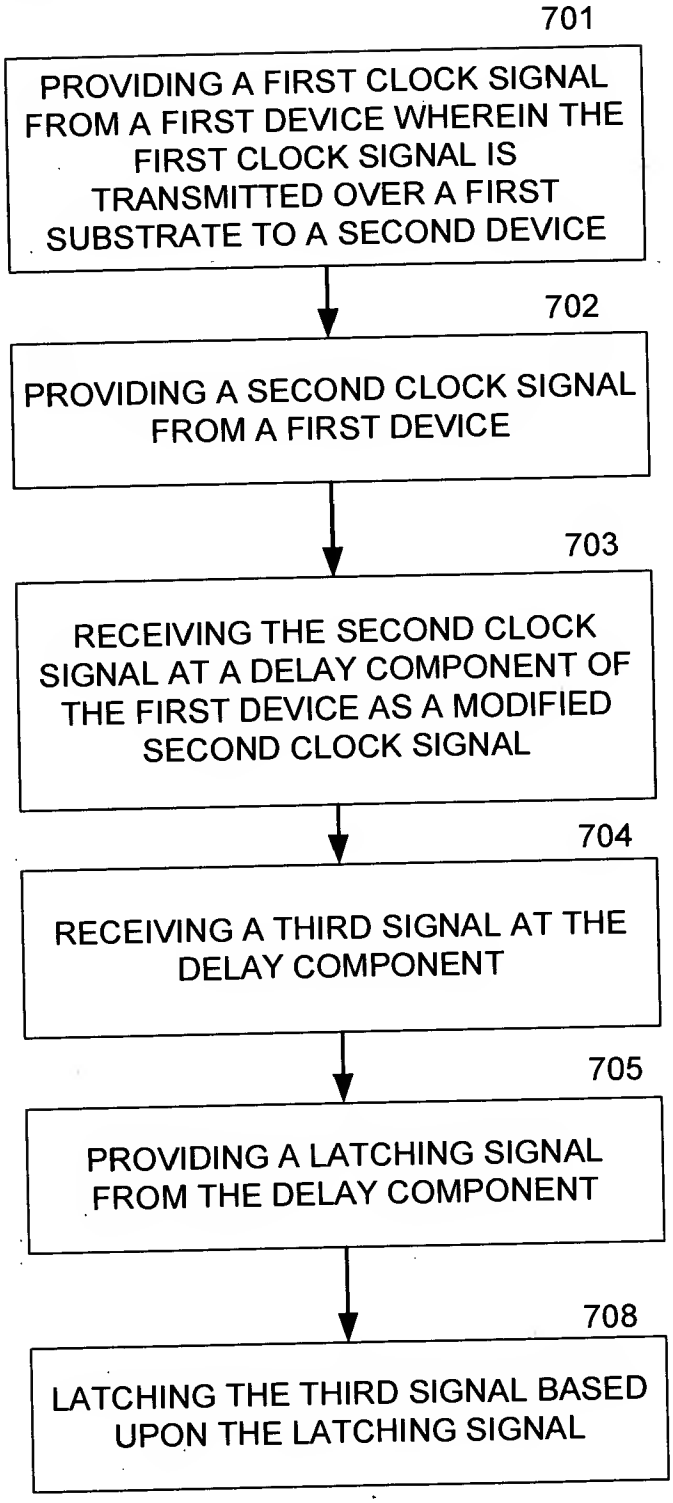
701
PROVIDING A FIRST CLOCK SIGNAL FROM A FIRST DEVICE WHEREIN THE FIRST CLOCK SIGNAL IS TRANSMITTED OVER A FIRST SUBSTRATE TO A SECOND DEVICE
702
PROVIDING A SECOND CLOCK SIGNAL FROM A FIRST DEVICE
703
RECEIVING THE SECOND CLOCK SIGNAL AT A DELAY COMPONENT OF THE FIRST DEVICE AS A MODIFIED SECOND CLOCK SIGNAL
704
RECEIVING A THIRD SIGNAL AT THE DELAY COMPONENT
705
PROVIDING A LATCHING SIGNAL FROM THE DELAY COMPONENT
708
LATCHING THE THIRD SIGNAL BASED UPON THE LATCHING SIGNAL

FIGURE 7